WIDEBAND HIGH GAIN SMALL SIZE MONOLITHIC GaAs FET AMPLIFIERS

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ABSTRACT

A series of two to four stage monolithic amplifiers operating with a gain of 15 to 42 dB and covering the 0.1 to 2 till 4 GHz frequency band has been realized. A high density of integration has been achieved (active area of 0.2 mm^2) as no decoupling capacitors nor inductances have been used.

INTRODUCTION

The broadband amplifiers used in the instrumentation, especially to increase the sensitivity of very high frequency dividers, should exhibit a gain of 30 to 40 dB or even more over several GHz. Some specific problems are related to this high amplification level.

1) While the required upper end of frequency band is determined by the performance of the divider (some 3 to 5 GHz), the low frequency limit is imposed by the amplifier itself : if D.C. coupling is used, the high D.C. gain makes difficult to control the biasing of the last stages ; the low frequency, 1/f type, noise of GaAs FET, when amplified, can saturate the output stage. The low frequency cut off is limited by the last consideration to around one hundred megahertz.

2) To achieve the desired amplification on a reasonably small area, a high gain density (100 to 150 dB/mm^2) is needed. For this reason, as well as to simplify the amplifier technology and approach as near as possible that of monolithic logic circuits, it is desirable to avoid the use of interstage blocking MIM capacitors and peaking inductors. This is possible by D.C. coupling techniques used in BFL circuits[1].

ACTIVE LOAD

To conciliate two contradictory requirements : the low frequency limitation of the band and the D.C. coupling, a frequency dependent active load has been used. It consists of a FET provided with a parallel/series negative feedback through a RC network (fig. 1). The capacitance of the feedback path is constituted by the FET input capacitance C_{gs}. However, if the RC product, which determines the low cut off frequency, is not large enough, an extra Schottky barrier capacitance can be added.

At frequencies much higher than 1/RC the circuit behaves as the classical gate-to-source-connected active load with load admittance $y_L = y_{ds} + y_{dg} + 1/R$. For $g_m \approx 12\ g_{ds}$ and a gate width of inverter twice as large as that of load FET, it results a voltage gain of about 18 dB.

At low frequencies, the circuit performs as a common drain stage with an output conductance $g_L \approx g_m$ which leads to nearly zero dB gain of the stage.

Another feature of this circuit is the biasing facility : the current of two transistors is imposed by the gate voltage of the amplifying FET, while the voltage across the transistors is determined mainly by the gate voltage of the load FET. Fig. 2 shows an example of the calculated regions of linear operation of amplifier. The allowed variation of V_g (for a given V_p) is to be compared with that of classical active load ($V_{gs2} = 0$).

AMPLIFIER DESIGN

The basic amplifier cell is composed of an amplifier stage with a 50 µm gate width common source transistor and 25 µm gate active load followed by a buffer/level-shifter stage which provides the D.C. coupling and the impedance transformation mainly to separate the load from the gate capacitance of the next cell.

Different amplifiers using two, three or four amplifier cells have been realized. To widen the bandwidth, a resistive feedback across one cell has been used.

The input matching has been achieved either by a parallel resistance included in the biasing circuit (as in the amplifier fig. 3b), or by a common gate input stage, with a 200 µm gate transistor (amplifier fig. 3a).

The output matching has been realized by two cascaded common drain stages with 100 µm and 200 µm gate width of the amplifying transistors.

The technology used to make these amplifiers has been the same as the one used for BFL gates[2]. In a next step, it will be possible to integrate the amplifier and logic circuits on the same chip.

The starting material has been an active layer doped by direct implantation of Selenium into a in-house CZ grown Cr doped GaAs substrate. The doping level has been 1.5 10^{17} at cm^{-3} and the

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pinch off voltage of 3 volts. The inactive areas have been made semi-insulating by a boron implantation. The FETs have been realized by the usual self-alignment method[3] with Al gate and AuGeNi source and drain. Then silicon dioxide has been deposited on the wafer, and finally a second level of metallisation made of TiPtAu deposited which makes the proper interconnections between elements.

The gate length is about 0.8 µm in a 2.5 µm drain-source spacing. The resistances have been made in the same time as FETs with N-GaAs channels provided with AuGeNi contacts. The capacitor used in the feedback circuit is a negatively biased Schottky-barrier diode, also made in the same time as FETs. Care has been taken in the design of the amplifier to keep the bias of this diode smaller than the pinch-off voltage of the N-layer.

A standard pad lay-out has been used for nine types of amplifiers with different complexity (fig. 4). Therefore, in this realisation, no special attention has been paid to attempt a very high density of implantation. Nevertheless, the active area for a multistage amplifier is already quite small.

RESULTS

Fig. 5 shows the typical frequency response of five types of amplifiers : three two stage amplifier with different types of matching circuits, one three stage amplifier and one four stage amplifier.

The last one, intended to drive the high input impedance frequency divider was not output matched. It performs a voltage gain of 42 dB. Despite of high gain level and small dimensions of the active area (0.6 to 0.3 mm), no instabilities due to internal parasitic feedback occurred.

The matching characteristics of the two stage amplifier A9 are shown in fig. 6.

The amplifiers have been biased typically at V_{dd} = 5 V, V_{ss} = - 3.5 V and V_p = 2.5 V. Due to the special load used, the biasing is not critical even for multistage amplifiers.

ACKNOWLEDGMENTS

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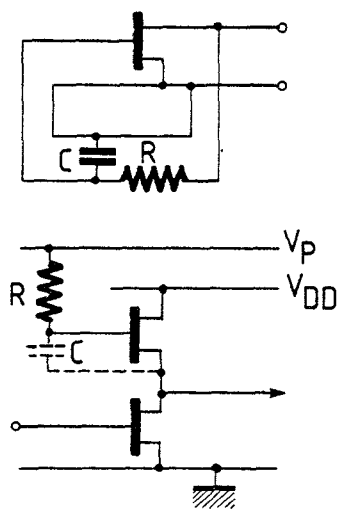


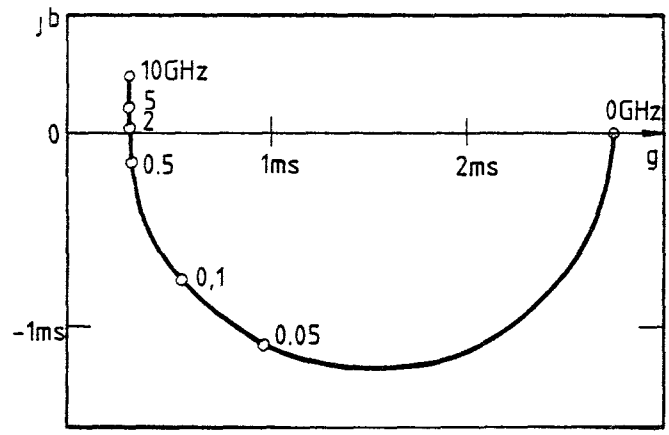


FIGURE 1 : High pass load
- principal feedback circuit
- amplifier stage with load
- calculated admittance of the load (W_{gate} = 25 um, R = 40 Kohm C_{total} = 0.12 pF)

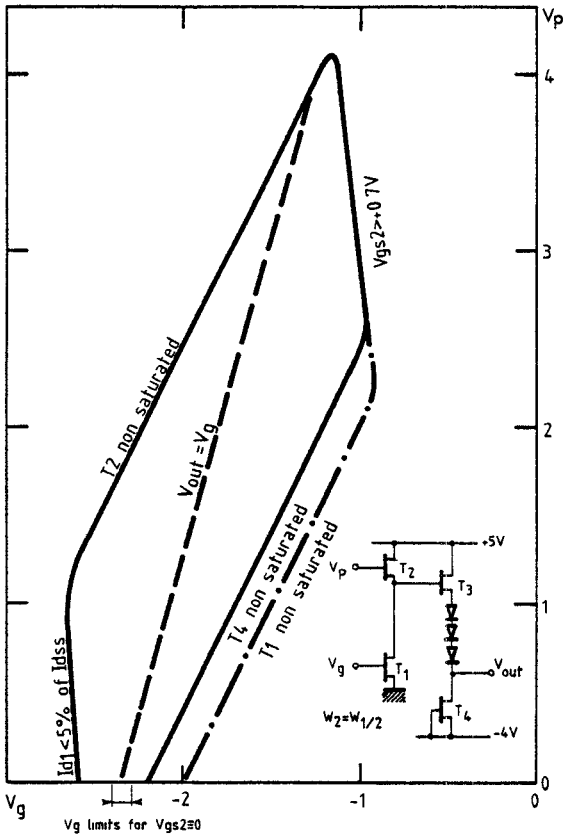
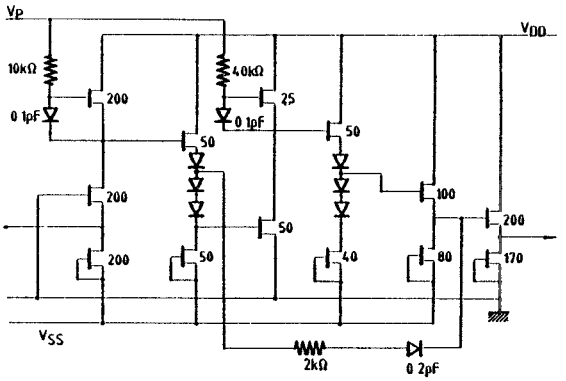
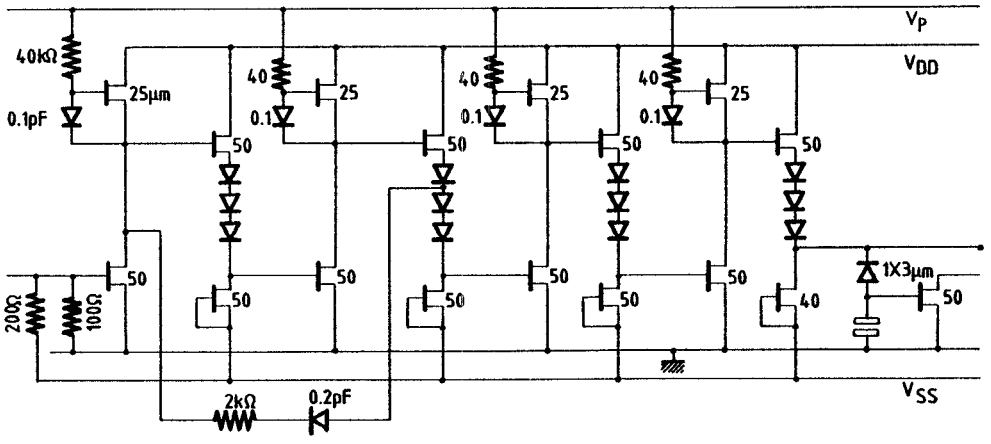


FIGURE 2 : The calculated limits (inner area) of the input and polarization dc voltages which maintain the amplifier cell biasing in the linear region.

- The dashed line is the loci of V_g and V_p for which no dc voltage shift through the amplifier occurs.
- Arrows on the bottom indicate the allowed V_g voltage gap, if T_2 is a gate-to-source-connected type active load.



(a)



(b)

FIGURE 3 :

Schematic of two amplifiers :

a) two stage input/ output active matched amplifier (A9)

b) four stage voltage amplifier (A6)

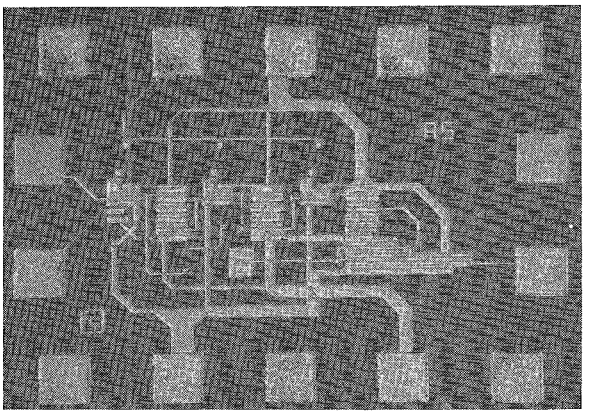


FIGURE 4 : Microphotograph of a three stage amplifier with two feedback loops (A5).

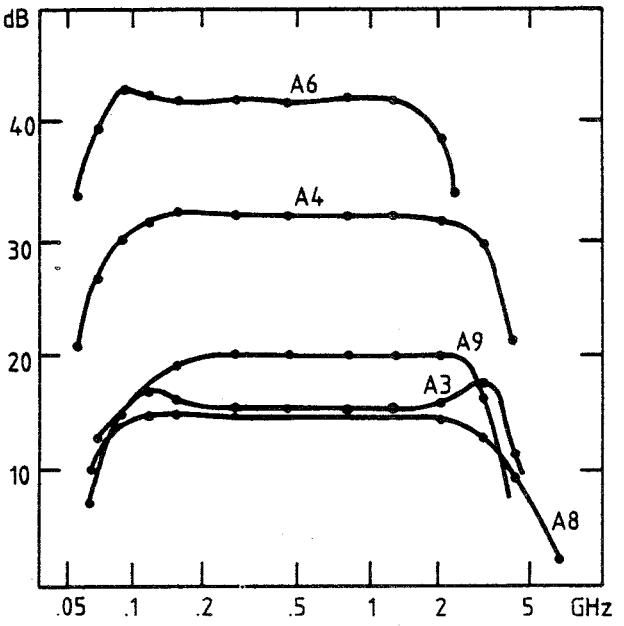


FIGURE 5 : Measured frequency responses of five amplifiers.

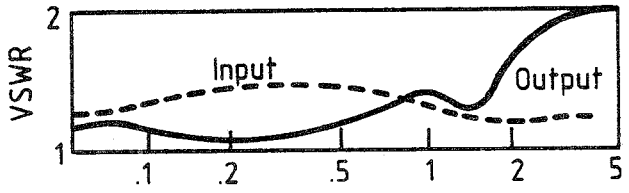


FIGURE 6 : Measured input/output matching characteristics of amplifier A9.